Claim 1 recites an integrator array of a plurality of integrators arranged in rows and columns respectively equal to said rows and columns of said photosensing array. See, e.g., FIGS. 1B and 1C and the associated textual description in the original specification for support.

In contrast, Pain discloses a linear array 30 of integrators 35 where the sensing pixels in one column of the APS array share a single integrator 35 connected to that column. Therefore, contrary to the contention made in the Office Action, Pain fails to disclose this aspect of Claim 1. Parker is entirely silent on this aspect of Claim 1. Therefore, the combination of Pain and Parker fails to disclose at least this aspect of Claim 1.

For this reason alone, Claim 1 is patentable over Pain and Parker.

In addition, Claim 1 further recites that "integrators of each column are coupled to receive electrical pixel signals from only one designated column of sensing pixels in said photosensing array and are operable to produce time-delayed integration signals representing the object after each sensing pixel is sampled and read out for a number of times equal to a number of said rows in said photosensing array." Pain and

Parker, either individually or collectively, fail to disclose this part of Claim 1. This further supports that Claim 1 is patentable.

Claims 2 and 4-11 are dependent claims of the base Claim 1 and thus are patentable over Pain and Parker for at least the above reasons.

Claims 12-15 stand rejected under 35 USC 102(a) as allegedly being anticipated by Pain. This contention, again, is traversed because Pain fails to disclose each feature of Claims 12-15.

Claim 12, which is the base claims for dependent Claims 13-15, recites an integrator array having m amplifiers electrically coupled to said m columns of active pixel sensors, respectively and each amplifier is coupled to n pairs of capacitors so that each pair of capacitors accumulate electrical pixel signals from n different active pixel sensors in a respective column that are generated at different times to produce a summed signal.

The Office Action contends that Pain teaches the recited n pairs of capacitors in the illustrated single pair of capacitors CMS and CMR in FIG. 2A. This contention, however, is based on a misunderstanding of the technical features in Pain.

Claim 12 recites that each amplifier is coupled to n pairs of capacitors. Notably, the number of the recited pairs of capacitors in Claim 12 is the same as the number of rows of active pixel sensors in the recited sensing array. As described in the original specification of the present application with reference to FIG. 2A, a total of n pairs of integrating capacitors (C-1 and C+1, C-2 and C+2, ..., C-n and C+n) are coupled to the two differential outputs 212a and 212b of the opamp 210 in FIG. 2A to form the array of n integrators for that column (page 15, lines 14-17 of the specification). This is one implementation of the integrator array 120 with n rows and m columns shown in FIG. 1B.

Pain, in contrast, discloses only one pair of capacitors CMR and CMR for each column of pixels and therefore fails to disclose this aspect of Claim 12. In FIGS. 1 and 2A, Pain specifically discloses that each column of APS pixels is connected to a single integrator 35. Therefore, Pain fails to disclose the above features in Claim 12.

Therefore, Claim 12 is patentable over Pain.

Claim 12 further recites that each pair of capacitors accumulate electrical pixel signals from n different active pixel sensors in a respective column that are generated at

different times to produce a summed signal. Pain, lacking any disclosure of the n integrators for each column of an APS array with m columns and n rows, fails to disclose this feature of Claim 12. This difference between Claim 12 and Pain further shows that Claim 12 is distinctly different from and is patentable over Pain.

Claims 16, 17 and 19 stand rejected under 35 USC 103(a) over Parker in view of Pain. Applicants respectively traverse.

Claims 16, 17, and 19 recite "spatially shifting the mapping from the sensing array to the integrator array in sampling the different frames along the predetermined direction to produce a summed signal that sums pixel signals from different pixel locations of different frames corresponding to a common image from a location on the object." The Office Action cites Col. 3 in Parker to show the teaching by Parker on this aspect. Parker, however, describes controlled charge transfer from one CCD pixel to another that is synchronized to the web advancement. The alleged combination of Parker and Pain cannot be properly made because Parker's CCD devices are known to transfer charge from one pixel to another for readout and Pain's APS arrays are specifically designed to avoid such intra-pixel charge transfer.

Notably, Claims 16, 17, and 19 recite the use of a linear sensing array and a linear integrator array for sampling the linear sensing array. Parker is completely silent on the use of such separate linear sensing array and the linear integrator array. Pain discloses a single integrator 35 connected to a column of APS sensing pixels in FIG. 1 and fails to disclose any use of an entire linear array of integrators in connection with a linear array of APS sensing pixels.

Based on the above, Parker and Pain, either individually or collectively, fail to disclose this aspect of Claims 16, 17, and 19. Hence, Claims 16, 17, and 19 are patentable.

Claim 18 is patentable under 35 USC 103(a) over Parker, Pain and Hosier based on the above arguments for Claim 17 because Hosier fails to fill the voids left by Parker and Pain.

In summary, all claims are distinctly patentable and the application should be in condition for allowance.

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Please apply a fee of $110 for extension of time for one month, and any other charges or credits, to Deposit Account No. 06-1050.

Respectfully submitted,

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